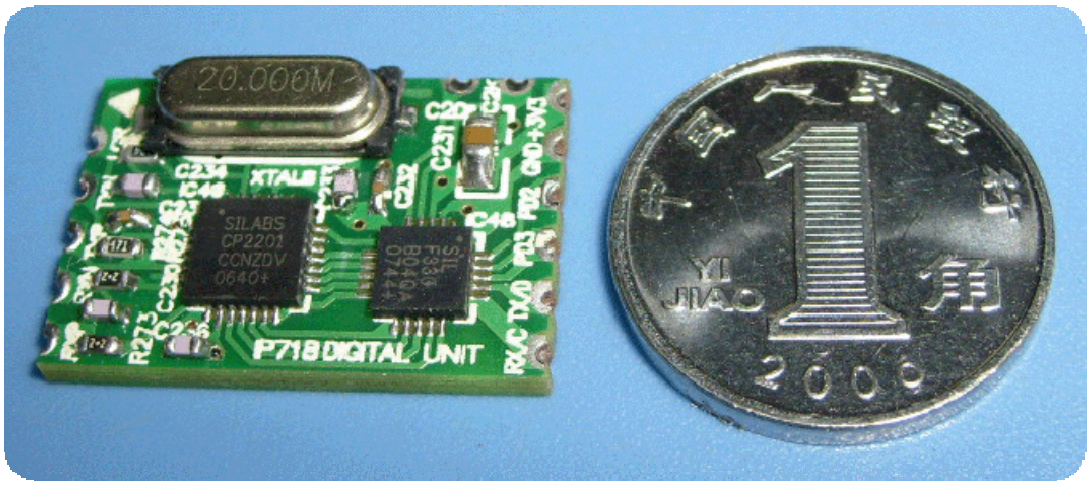
IP71B Ethernet Singlechip Interface Converter User Manual

Using Ethernet network to carry out long distance control is the development direction of various fields such as industrial control, security-monitoring, etc. users can utilize perfect network communication platform to realize the equal communication between products. IP71B is easy to access to Ethernet, and can choose various communication modes such as I^2C, SPI, and UART. The least only need two ordinary IO ports.

◆ Characteristics

- ✧ Industrial level 10base-T Ethernet interface, compatible with 100M/1000M/10G networks.
- ✧ Built-in I^2C slave interface can connect with the ordinary IO port of any single chip. Users have the initiative to modify I^2C address.
- ✧ User single chip can use ordinary IO port software to simulate I^2C interface. I^2C can control IP71B and connect in parallel other I^2C standard devices. There is no need to use additional I^2C interface.
- ✧ The INT pin of open-drain output INT pin turns to low to remind users' single chip carrying out read I^2C operation when users receive the valid data packet of Ethernet.
- ✧ Built-in SPI slave interface. Can choose SPI interface when the data speed request of transmission is fast. User single chip also can use ordinary IO port to simulate SPI time sequence.
- ✧ Built-in UART standard interface uses TXD port and RXD port, and support 300 to 115200BPS transmission speed.
- ✧ Built-in 10-bit precision sensor can read the working temperature of IP71B through Ethernet or user mainframe.
- ✧ Adopt 3.3V single power supply, built-in independent watchdog.
- ✧ Using Winsocker to program is simpler than RS232 and LPT, and transmission speed is faster.
- ✧ Internal 4KB receiving buffer and 2KB sending buffer, communication mode is more unrestricted.



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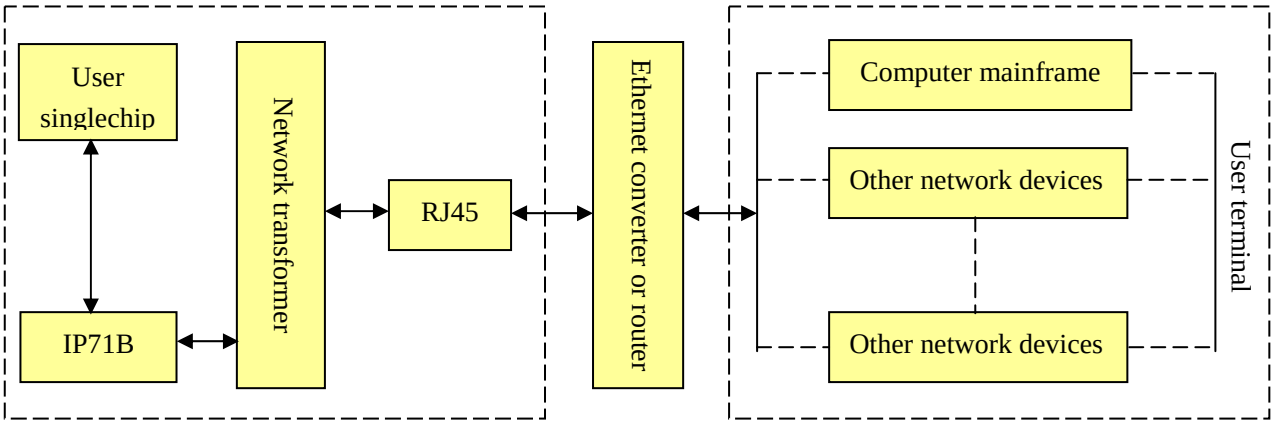
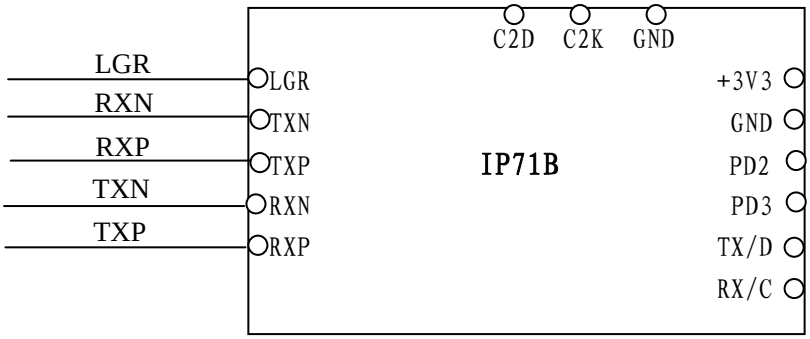
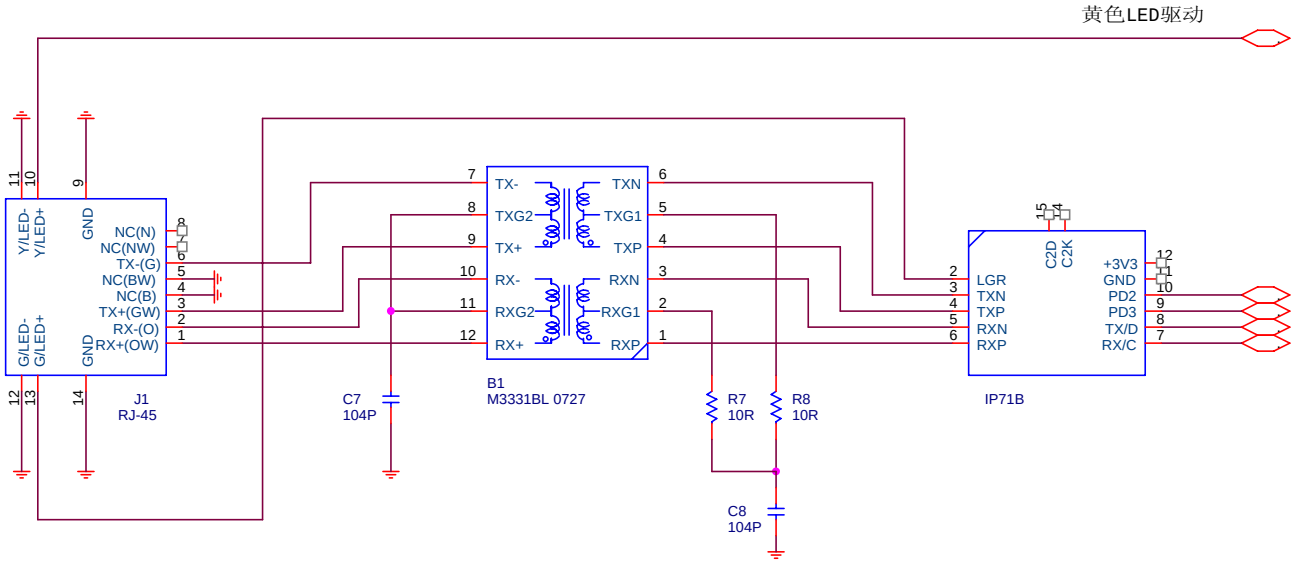


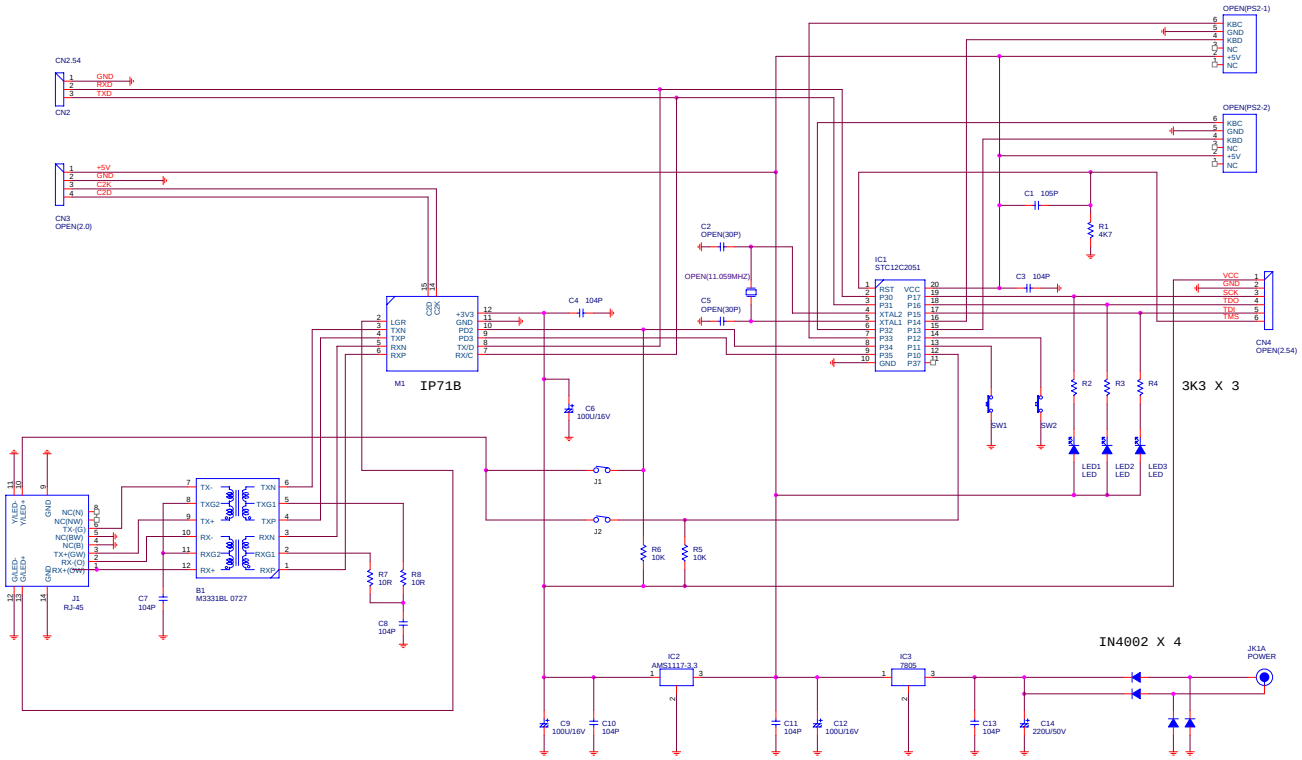
IP71B typical application block diagram

Note: in practical use, it is acceptable that users don't adopt converter and router; if so, the network interface pins connections are as follows.

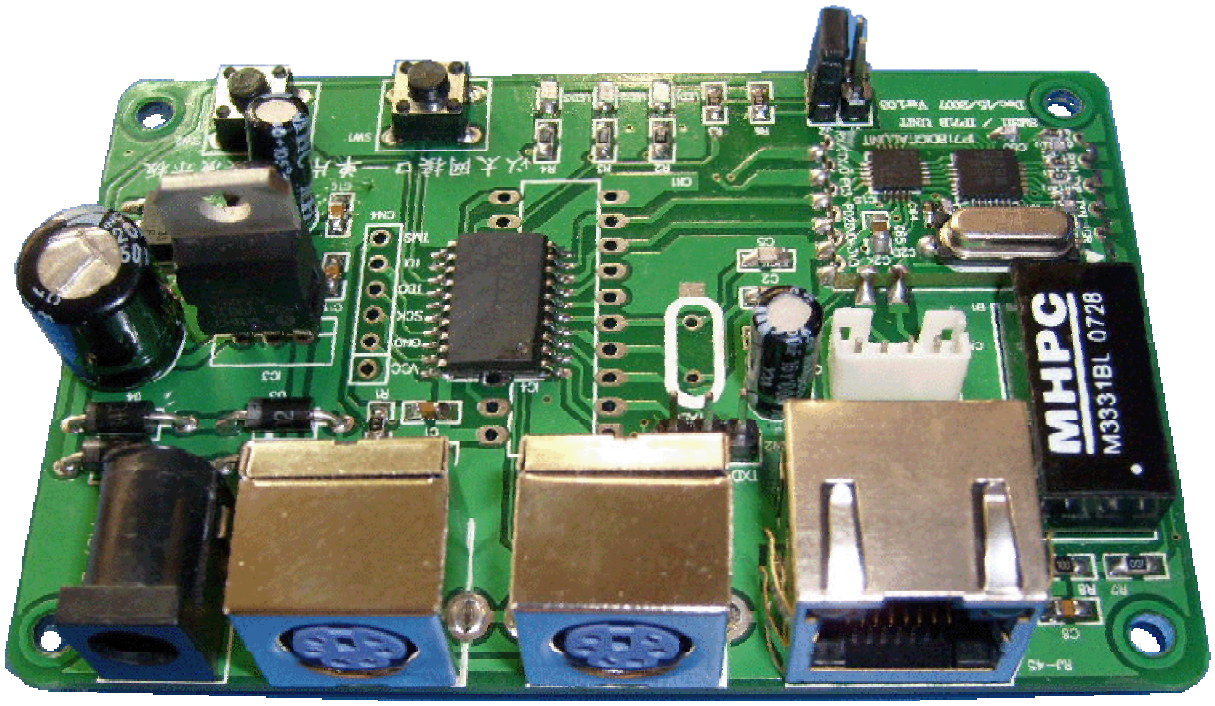




IP71B Ethernet terminal network transformer and RJ45 interface connection diagram



Ethernet-singlechip interface connection Demonstration board

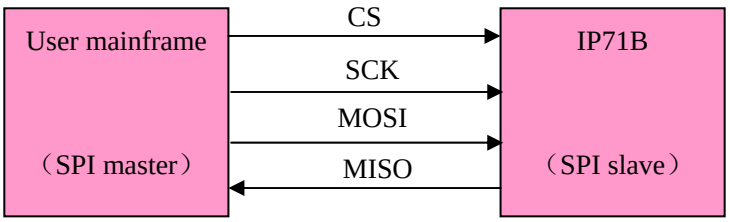


◆ The files relating to IP71B

- 《IP71X Ethernet Interface communication protocol》----------hsavd110.pdf
- 《ST-991AR5 upgrade device user manual》----------cnstl201.pdf

◆ SPI bus application instructions

SPI bus connecting with user mainframe is supported by IP71B, and using four ordinary IO ports is okay, as shown in the following illustration.



The diagram using SPI to connect user mainframe with IP71B

SPI bus consists of CS, SCK, MOSI, and MISO. If user mainframe has not built-in SIP control, can use software mode to generate SPI time sequence. When user mainframe system has many devices of SPI bus can connect in parallel SCK, MOSI, and MISO with the SCK, MOSI, and MISO of IP71B. When CS is high, the MISO of IP71B is high-resistance state. For the standard SPI device, all MISO are high-resistance state when CS chip selection is noneffective.

When use SPI bus, the yellow LED light of RJ45 interface will be controlled by user mainframe. User mainframe regularly uses MOSI to write Ox00, when the value read is not Ox00 means that IP71B has received the data packet sent by server. When MISO is Ox01 have a package of data packet that has not been read, When MISO is Ox02 have two packages of data packets that have not been read, and the rest may be deduced by analogy. After CS chip selection turns to low, sending the Oxff of one byte later will turn into high CS, and it is a read state register, after finishing, CS will turn to high, and return to the idle state of SPI. User mainframe writes Ox00 and prepares to read the data of MISO after CS turns to low, the value of MISO read by the first byte is the counter of packet that has not been read, at this time, must keep CS low until all bytes have been read completely.

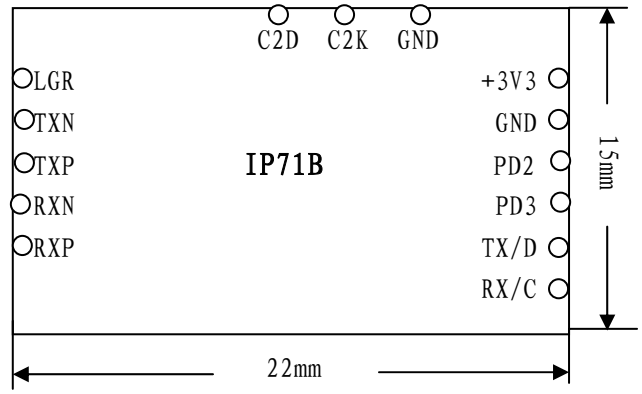
The second byte is the length of instruction packet, and accords with the length of instruction set; its valid value is Ox02 to 138. User mainframe reads all bytes according to the value of length. The value sent by MOSI should be Oxff while reading.

When user mainframe needs to send data packet, the first byte is length that the valid value is 2 to 138, and accords with the length of instruction set. User mainframe must write instruction packet data that is same as length.

When the first byte turning to low in the CS is oxff means that user mainframe does not read the state of instruction packet, if it is Ox00 means that user mainframe reads instruction packet, and it is Ox02 to Ox8a means that user mainframe sends instruction packet. When only have oxff, CS is an 8-bit time and low, after finishing it will turn into high CS. CS will become high after finishing read and writing while reading and sending instruction packet.

The highest clock of SPI clock is 6MHz. So the maximum value of communication speed adopting SPI is 6Mbps.Comparing with I^2C and UART, this speed is the highest. If system has SPI components or user mainframe has system IO can have priority in using SPI bus to get faster communication speed.

◆ Instructions of pins



Note: see under for module interface and dimension diagram.

LGR LED connection signal output.

TXN Ethernet transformer sending-terminal negative port.

TXP Ethernet transformer sending-terminal positive port.

RXN Ethernet transformer receiving-terminal negative port.

RXP Ethernet transformer receiving-terminal positive port.

C2D Module firmware upgrading and simulation port. In general, user may pay attention to it unnecessarily.

C2K Module reset input. In general, user may pay attention to it unnecessarily.

GND Ground wire input/output.

+3V3 Power supply+3.3V.

GND Ground wire input/output.

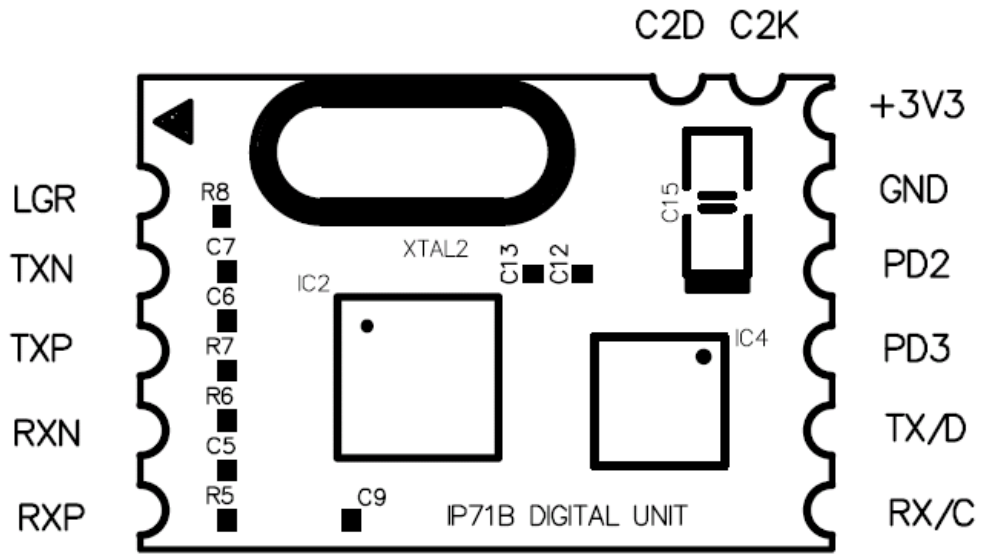
PD2 This port is Ethernet yellow LED drive output when choose I^2C and UART communication mode, and it is used to indicate the state of power supply and data communication. This port is SCK clock input port when choose SIP communication mode.

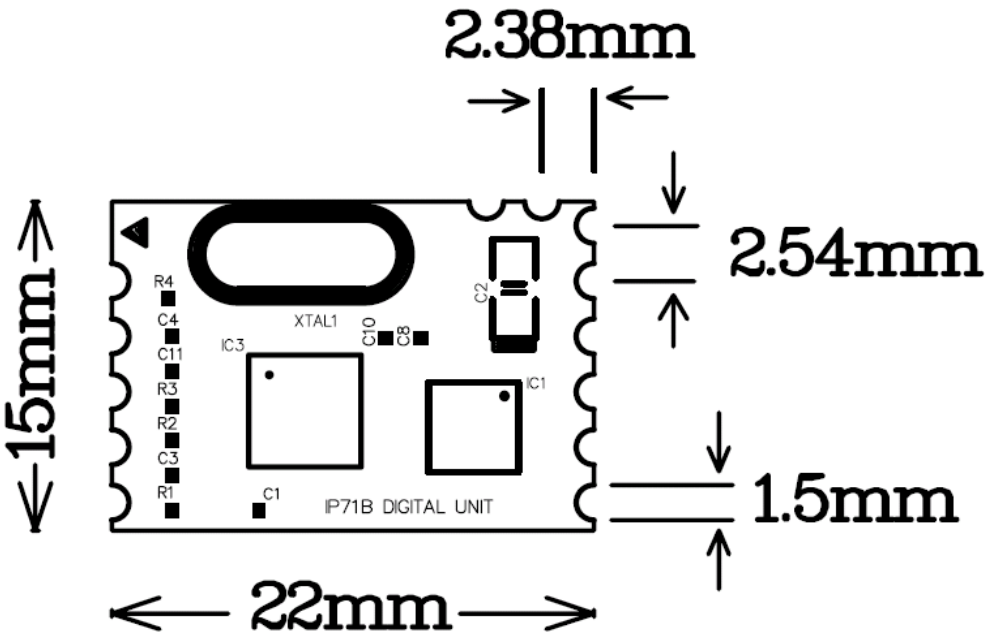
PD3 This port is INT output when choose I^2C communication mode. Turn to low when have data to need user single chip to read, and return to high-resistance input after finishing. NC is not used when choose UART communication mode. This port is MISO data terminal output terminal when choose SPI communication mode.

TX/D It is SDA data input/output terminal when choose I^2C communication mode. It is TXD data output when choose UART communication mode, and connects with the RXD terminal of single chip. It is MOSI data input when choose SPI communication mode, and connects with the data input of user single chip (SPI mainframe).

RX/C It is SCL clock input when choose I^2C communication mode, and connects with the I^2C clock output of single chip. It is RXD data input when choose UART communication mode, and connects with the TXD terminal of user single chip. It is CS chip selection pin input when choose SPI communication mode, and connects with single chip SPI chip selection output terminal.

Note: All ports output 3.3V level and can input 5 V level. There is no need for connecting 5V singlechip to do any conversion.





◆ Ethernet interface RJ45 connector instruction

The color code and arrangement method of twisted-pair have the unified international standards, now TIA/EIA568B is in common use. AMP twisted-pair consists of 8 lines; and is divided into 4 pairs, each pair is a pair of twisted-pair, i.e. (orange, white/orange), (green, white/green), (brown, white/brown), (blue, white/blue). If twisted-pair is used to connect with hub, the arrangement mode of connector pins is as follows. (TIA/EIA568B)

1->orange-white

2->orange

3->green-white

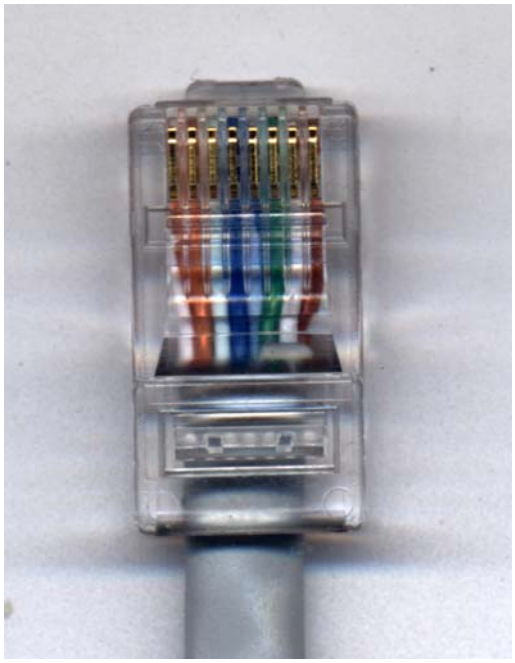
4->blue

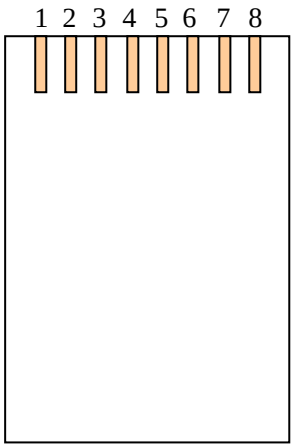
5->blue-white

6->green

7->brown-white

8->brown





Connector front view and pins sequence

One group of signal will be transmitted through two core lines that are not intertwisted together while using cable two-end one-to-one connections mode, which can generate the strong next-near-end-crosstalk. So users have to arrange twisted-pair according to the international standards.

RJ45 connector twisted-pair definition is as follows：(10BaseT, 100BaseTX)

1 Rx+

2 Rx-

3 Tx+

6 Tx-

Note: 4, 5, 7, 8 are empty pins; 1, 2 are used for sending; 3, 6 are used for receiving; 4, 5, 7, and 8 are bi-directional lines.

2、If users don't adopt hub in practical use, the arrangement mode of connector pins is as follows.

3->green-white

6->green

1->orange-white

4->blue

5->blue-white

2->orange

7->brown-white

8->brown

◆ Electrical specifications

Item	Minimum	Normal	Maximum	Unit
Voltage	3.1	3.3	3.6	V
Current (Have network connection)	—	125	155	mA
Current (Don't have network connection)	—	73	—	mA
Temperature	－40	—	＋85	℃